

WHAT IS CLAIMED IS:

1. A non-volatile semiconductor memory device, comprising:
 - a semiconductor substrate comprising a device active area and a device isolation area;
 - a control gate on the device active area, wherein the control gate divides the device active area into a first region and a second region;
 - a control gate insulating layer between the substrate and the control gate;
 - a first insulating layer covering a top surface and a side of the control gate;
 - a drain region in the first region of the substrate;
 - a source region in the second region, wherein the source region is separated from the control gate;
 - a second insulating layer formed on the second region between the source region and the control gate and formed on a portion of a surface of the first region adjacent the first insulating layer and over the drain region; and
 - a floating gate covering the second insulating layer and the first insulating layer.
2. The device according to claim 1, further comprising a third insulating layer over the floating gate.

3. The device according to claim 2, wherein the first and the third insulating layers comprise high etch selectivity materials.

4. The device according to claim 2, wherein the first and second insulating layers are formed of silicon oxide and the third insulating layer is formed of silicon nitride.

5. The device according to claim 1, wherein the floating gate extends into both the first and second regions and overlaps the control gate.

6. The device according to claim 1, further comprising:
an insulating interlayer covering the device active area including a surface of the floating gate;
a contact hole in the insulating interlayer, wherein the contact hole exposes
5 a portion of the drain region where the floating gate is not located; and
a bit line over the insulating interlayer, wherein the bit line is coupled to the drain region through the contact hole.

7. The device according to claim 6, further comprising a fourth insulating layer covering the second region, the floating gate, and the first region where the floating gate is not formed.

8. The device according to claim 1, wherein the source region and drain regions are formed to asymmetrically center around the control gate.

9. A non-volatile semiconductor memory device, comprising:

a plurality of device active areas extending along a first direction separated from one another in parallel on a semiconductor substrate each having a plurality of memory cell areas;

5 a plurality of control gates crossing over the device active areas, wherein each of the plurality of control gates are separated from one another in a second direction crossing the first direction to determine the memory cell areas;

a plurality of drain regions in the device active areas located on a first side of each of the plurality of control gates;

10 a plurality of source regions in the device active areas located on a second side of said each of the plurality of control gates opposite from the drain regions; and

a plurality of floating gates that overlap the control gates, portions of the drain regions, and portions of the device active areas, wherein the plurality of floating gates do not overlap the source regions formed at the second sides of the control gates.

10. The device according to claim 9, wherein the plurality of device active areas are separated from one another in parallel by a plurality of device isolation layers.

11. The device according to claim 9, wherein each of the plurality of source regions are separated from the control gates.

5 12. The device according to claim 9, further comprising a plurality of control gate insulating layers between the control gates and the device active areas of the semiconductor substrate.

13. The device according to claim 9, further comprising:
a plurality of bit line contacts at portions of the drain regions that do not
10 overlap the floating gates in the memory cell areas; and
a plurality of bit lines, wherein the bit lines are in contact with the bit line contacts, overlap the device active areas and extend in the first direction.

14. The device according to claim 13, wherein the plurality of bit lines are isolated from one another by an insulating interlayer on the device active areas.

15. The device according to claim 9, wherein the floating gates are isolated from the control gates by inter-polysilicon layers.

16. The device according to claim 15, further comprising a plurality of sidewall spacers formed of an insulating material inserted between lateral sides of the inter-polysilicon layers and the floating gates.

17. The device according to claim 16, wherein the insulating material comprises
5 a nitride.

18. A method of fabricating a non-volatile semiconductor memory device, comprising:
forming a control gate on a portion of a memory cell area of a semiconductor substrate, wherein the memory cell area, which is divided into a first
5 region and a second region by the control gate, is defined by a device isolation layer;
providing a control gate insulating layer between the control gate and the semiconductor substrate;

- forming a first insulating layer on an exposed surface of the control gate;
forming a drain region in the first region;
- 10 forming a third insulating layer covering portions of the second region and
the drain region, wherein the third insulating layer is extended from the first insulating
layer;
- forming a floating gate on the third insulating layer and on an exposed
surface of the first insulating layer; and
- 15 forming a source region in the second region, wherein the floating gate does
not overlap the source region.

19. The method according to claim 18, wherein the control gate is formed of
doped polysilicon and the first insulating layer is formed by oxidizing a surface of the
doped polysilicon.

20. The method according to claim 18, wherein the forming of the drain region
comprises:

- forming an ion-implantation mask that exposes only the first region;
 doping the exposed first region with impurities; and
- 5 removing the ion-implantation mask.

21. The method according to claim 18, further comprising forming a second insulating layer on a surface of the first insulating layer at a side of the control gate wherein the etch selectivity of the second insulating layer differs from the etch selectivity of the first insulating layer.

22. The method according to claim 18, wherein the control gates are formed to extend to other memory cell areas adjacent to the memory cell area.

23. The method according to claim 18, wherein the forming of the third insulating layer and the floating gate comprise:

forming an oxide layer on the exposed surface of the first region;

forming a tunneling oxide layer on the second region of the substrate;

5 forming a conductive layer over the substrate including the oxide layer, the tunneling oxide layer, and the first insulating layer; and

patterning the conductive layer, the oxide layer and the tunneling oxide layer to overlap the control gate and portions of the drain and source regions.

24. The method according to claim 23, wherein the tunneling oxide is formed by thermally oxidizing an exposed surface of the second region of the substrate.

25. The method according to claim 23, wherein the conductive layer comprises doped polysilicon, wherein the portion of the drain overlapped by the floating gate is greater than the portion of the source overlapped by the floating gate.

26. The method according to claim 18, further comprising:
forming an insulating interlayer over the semiconductor substrate including the floating gate;
forming a contact hole exposing a portion of the drain region that is not
5 covered with the floating gate by removing a portion of the insulating interlayer; and
forming a bit line on the insulating interlayer, wherein the bit line fills up the contact hole and forms a plug coupled to the bit line.

27. The method according to claim 18, further comprising forming a fourth insulating layer on exposed surfaces of the floating gate and the first and second regions of the semiconductor substrate.

28. The method according to claim 27, wherein the fourth insulating layer is formed by oxidizing exposed surfaces of the floating gate and the first and second regions of the semiconductor substrate.

29. A method of fabricating a non-volatile semiconductor memory device,
comprising:

forming a control gate on a portion of a memory cell area of a
semiconductor substrate, wherein the memory cell area, which is divided into a first
5 region and a second region by the control gate, is defined by a device isolation layer;

inserting a control gate insulating layer between the control gate and the
semiconductor substrate;

forming a first insulating layer on an exposed surface of the control gate;

forming a second insulating layer on a surface of the first insulating layer at
10 a side of the control gate, wherein the etch selectivity of the second insulating layer differs
from the etch selectivity of the first insulating layer;

forming a drain region in the first region adjacent the control gate;

forming an oxide layer on an exposed surface of the first region and a
tunneling oxide layer on the second region of the substrate;

15 forming a conductive layer over the substrate including the oxide layer, the
tunneling oxide layer, and the first insulating layer;

forming a source region in the second region; and

forming a floating gate and a third insulating layer by patterning the
conductive layer, the oxide layer and the tunneling oxide layer to overlap the control gate

20 and portions of the drain region and a source junction, wherein the floating gate does not overlap the source region.

30. The method according to claim 29, wherein the control gate is formed of doped polysilicon and the first insulating layer is formed by oxidizing a surface of the doped polysilicon.

31. The method according to claim 29, wherein forming the drain region comprises:

forming an ion-implantation mask exposing only the first region on the semiconductor substrate;

5 doping the exposed first region with impurities; and
removing the ion-implantation mask.

32. The method according to claim 29, wherein the control gates are formed to extend to other memory cell areas adjacent to the memory cell area.

33. The method according to claim 29, wherein the source region is separated from the control gate by a prescribed distance and the oxide region is thicker than the tunneling oxide layer.

34. The method according to claim 29, further comprising:
5 forming an insulating interlayer over the semiconductor substrate including the floating gate;
forming a contact hole exposing a portion of the drain region that is not under the floating gate, by removing a portion of the insulating interlayer; and
forming a bit line on the insulating interlayer, wherein the bit line fills up
10 the contact hole and forms a plug that is connected to the bit line.

35. The method according to claim 29, further comprising forming a fourth insulating layer on exposed surfaces of the floating gate and the first and second regions of the semiconductor substrate.

36. A method of preventing disturbance of a non-volatile semiconductor
5 memory comprising:
providing a non-volatile semiconductor memory device comprising a plurality of memory cells each of which comprises a control gate, a drain junction, a source junction, a floating gate, a word line, and a bit line;
generating a first electric charge of a first parasitic capacitance from an
10 applied control gate voltage and a floating gate voltage as a function of the first parasitic

capacitance with respect to the difference between the control gate voltage and the floating gate voltage;

generating a third electric charge of a third parasitic capacitance from a source voltage at the source junction and the induced floating gate voltage as a function
15 of the third parasitic capacitance with respect to the difference between the source voltage and the floating gate voltage;

generating a fourth electric charge of a fourth parasitic capacitance from a bulk substrate voltage and the induced floating gate voltage as a function of the fourth parasitic capacitance with respect to the difference between the bulk substrate voltage and
20 the floating gate voltage;

generating a second electric charge of a second parasitic capacitance from a drain voltage at the drain junction and the induced floating gate voltage as a function of the second parasitic capacitance with respect to the difference between the drain voltage and the floating gate voltage;

25 selecting one of the control gate voltage and the drain voltage to reduce disturbance at the word line and the bit line where the floating gate voltage is determined by the capacitance of the first and second parasitic capacitors, the control gate voltage, the drain voltage and the total parasitic capacitance; and

programming said non-volatile semiconductor memory by F-N tunneling
30 or erasing by discharging electrons.

37. The method according to claim 36, wherein the selecting is performed by providing a known one of the control gate voltage and the drain voltage and varying the other of the control gate voltage and the drain voltage to achieve the prescribed induced floating gate voltage.

38. The method according to claim 36, wherein said programming is done by F-N tunneling, wherein the F-N tunneling comprises using a voltage difference between the floating gate and the source junction and a channel region at a side of the source junction, thereby injecting electrons into the floating gate.

39. The method according to claim 36, wherein said programming is done by erasing, wherein said erasing comprises discharging electrons accumulated in the floating gate in use of F-N tunneling which uses voltage difference between the floating gate and a lateral side of the source junction, and wherein the erasing is achieved by selecting selected voltages for the control gate and the source not to discharge the electrons into the source junction due to a voltage applied to other memory cells sharing the word line.

40. The method of preventing disturbance of a non-volatile semiconductor memory according to claim 36, wherein the floating gate voltage is a function of the first through fourth parasitic capacitors with respect to the voltages of the control gate, drain,

source and bulk substrate and the total parasitic capacitance when a total of the electric
5 charges of the first to fourth parasitic capacitances is substantially equal to 0 and when the
floating gate at neutral and wherein the total parasitic capacitance is the sum of the first
through fourth parasitic capacitors.

41. The method of preventing disturbance of a non-volatile semiconductor memory according to claim 36, wherein the floating gate voltage V_{fg} is substantially equal to $(C_1V_{cg} + C_2V_d + C_3V_s + C_4V_b)/C_{total}$ as a total of the electric charges of the first to fourth parasitic capacitances $(Q_1 + Q_2 + Q_3 + Q_4)$ and is substantially equal to 0 when the floating gate at neutral, and wherein a total capacitance C_{total} is substantially equal to $(C_1 + C_2 + C_3 + C_4)$, wherein V_{cg} is the control gate voltage, V_d is the drain voltage, V_s is the source voltage and V_b is the bulk substrate voltage.

42. The method of preventing disturbance of a non-volatile semiconductor memory according to claim 36, wherein each of the non-volatile memory cells comprises:

a semiconductor substrate comprising a device active area and a device isolation area;

a control gate on the device active area, wherein the control gate divides the device active area into a first region and a second region;

a control gate insulating layer is inserted between the substrate and the control gate;

a first insulating layer covering a top surface and a side of the control gate;

a drain region in the first region of the substrate;

a source region in the second region, wherein the source region is separated from the control gate;

a second insulating layer formed on the second region between the source region and the control gate and formed on a predetermined portion of a surface of the first region between the first insulating layer and the drain region; and

a floating gate covering the second insulating layer and the first insulating layer.